CLAIMS

1. Edge illuminated epilayer waveguide phototransistor comprising:

a subcollector layer formed of an epitaxially grown quaternary semiconductor;

a collector region epitaxially grown on the subcollector layer;

a base region epitaxially grown on the collector layer;

an emitter region epitaxially grown on the base layer; and

the subcollector layer, the collector region, the base region, and the emitter region being formed so as to define an edge illuminated facet for receiving incident light.

2. Edge illuminated epilayer waveguide phototransistor as claimed in claim 1 wherein the subcollector layer is epitaxially grown on an InP substrate.

3. Edge illuminated epilayer waveguide phototransistor as claimed in claim 2 wherein the subcollector layer is composed of InGaAsP.

4. Edge illuminated epilayer waveguide phototransistor as claimed in claim 3 wherein the InGaAsP subcollector layer includes a composition that is transparent at the optical wavelengths of interest.

5. Edge illuminated epilayer waveguide phototransistor as claimed in claim 4 wherein the InGaAsP subcollector layer includes a InGaAsP composition that corresponds to a band gap wavelength of 1.15 μm.

6. Edge illuminated epilayer waveguide phototransistor as claimed in claim 1 wherein the subcollector layer has a thickness in a range of approximately 0.80 μm to 0.90 μm.

7. Edge illuminated epilayer waveguide phototransistor as claimed in claim 6 wherein the subcollector layer is doped to provide a sheet resistance value in a range of 20 Ω/square to 30 Ω/square.

8. Edge illuminated epilayer waveguide phototransistor as claimed in claim 1 wherein the collector region includes an

undoped InGaAs layer with a thickness chosen to optimize the transit frequency, breakdown voltage, base-collector capacitance, and rate of optical absorption.

9. Edge illuminated epilayer waveguide phototransistor as claimed in claim 8 wherein the collector region thickness is in a range of 0.3 μm to 0.5 μm.

10. Edge illuminated epilayer waveguide phototransistor as claimed in claim 8 wherein the collector region thickness is approximately 0.4 μm.

11. Edge illuminated epilayer waveguide phototransistor as claimed in claim 8 wherein the collector region thickness is chosen to provide a transit frequency of approximately 130 GHz.

12. Edge illuminated epilayer waveguide phototransistor as claimed in claim 8 wherein the collector region has a length selected to provide an internal quantum efficiency greater than 90%.

13. Edge illuminated epilayer waveguide phototransistor as claimed in claim 1 wherein the base region includes a doped base layer and an undoped spacer layer.

14. Edge illuminated epilayer waveguide phototransistor as claimed in claim 13 wherein the collector region is undercut below the base region, reducing the width of the collector region to minimize base-collector capacitance.

15. Edge illuminated epilayer waveguide phototransistor as claimed in claim 3 wherein the emitter region includes a layer of InGaAsP and a layer of InP.

16. Edge illuminated epilayer waveguide phototransistor as claimed in claim 15 wherein the layer of InGaAsP has a thickness in a range of approximately 0.05 μm to 0.15 μm.

17. Edge illuminated epilayer waveguide phototransistor as claimed in claim 16 wherein the InP emitter layer has a thickness large enough to prevent optical absorption loss in the top InGaAs emitter contact layer.

18. Edge illuminated epilayer waveguide phototransistor as claimed in claim 17 wherein the InP emitter layer has a thickness of approximately 0.5 μm.

19. Edge illuminated epilayer waveguide phototransistor as claimed in claim 15 wherein the emitter region further includes a contact layer of InGaAs.

20. Edge illuminated epilayer waveguide phototransistor comprising:

a subcollector layer formed of doped InGaAsP with a thickness in a range of 0.80 μm to 0.90 μm;

a collector layer of undoped InGaAs with a thickness in a range of 0.3 μm to 0.5 μm epitaxially grown on the subcollector layer;

a base region including a doped InGaAs layer epitaxially grown on the collector layer having a thickness of approximately 0.05 μm and an undoped InGaAs layer having a thickness of approximately 50 Å, epitaxially grown on the doped InGaAs layer;

an emitter region including a doped InGaAsP layer having a thickness in a range of 0.05 μm to 0.15 μm and epitaxially grown on the undoped InGaAs layer of the base region, a doped InP layer having a thickness in a range of 0.3 μm to 0.7 μm epitaxially grown on the doped InGaAsP layer, and a doped InGaAs emitter contact layer epitaxially grown on the doped InP layer; and

the subcollector layer, the collector layer, the base region, and the emitter region being formed so as to define an edge illuminated facet for receiving incident light.

21. Edge illuminated epilayer waveguide phototransistor as claimed in claim 20 wherein the subcollector layer, the collector layer, the base region, and the emitter region define a mesa having a width in a range of 1.0 μm to 5.0 μm and a length long enough to achieve a greater than 90% internal optical absorption efficiency.

22. A method of fabricating an edge illuminated epilayer waveguide phototransistor comprising the steps of:

providing a semiconductor substrate defining a surface;

epitaxially growing a subcollector layer formed of a quaternary semiconductor material on the semiconductor substrate;

epitaxially growing a collector region on the subcollector layer;

epitaxially growing a base region on the collector layer;

epitaxially growing an emitter region on the base layer; and

forming the subcollector layer, the collector region, the base region, and the emitter region to define an edge illuminated facet for receiving incident light.

23. A method as claimed in claim 22 wherein the step of epitaxially growing the subcollector layer includes growing the subcollector layer with a quaternary composition that

corresponds to a band gap wavelength that is transparent to the optical wavelengths of interest.

24. A method as claimed in claim 22 wherein the step of epitaxially growing the base region includes the step of growing a doped base layer on the collector layer and an undoped spacer layer on the base layer.

25. A method as claimed in claim 24 including the steps of etching the collector region to expose a surface portion of the undoped spacer layer, depositing a base metal electrode on the exposed surface portion, and using the base metal electrode as a mask, undercutting the collector layer to reduce base-collector capacitance.